UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,880,099 B1
DATED : April 12, 2005
INVENTOR(S) : Hai Thanh Nguyen et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 8,
Line 23, "reset signal (**706**, RS1)." should read -- reset signal (**706** RST) --.

Column 10,
Line 47, "Since many embodiment" should read -- Since many embodiments --.
Line 58, "pulse width that are" should read -- pulse width that is --.

Column 11,
Line 37, "a timing delay circuit is arranged" should read -- a timing delay circuit arranged --.
Line 41, "a comparator circuit is arranged" should read -- a comparator circuit arranged --.
Line 44, "a sampling logic is arranged" should read -- a sampling logic arranged --.

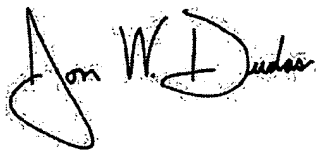
Column 12,
Line 29, "a timing delay circuit is arranged" should read -- a timing delay circuit arranged --.
Line 33, "a comparator circuit is arranged" should read -- a comparator circuit arranged --.
Line 36, "a sampling logic is arranged" should read -- a sampling logic arranged --.

Column 13,
Line 9, "a digital representation the of" should read -- a digital representation of --.

Column 14,
Line 5, "and an other logic" should read -- and another logic --.
Line 18, "data point in response the" should read -- data point in response to the --.

Signed and Sealed this

Sixteenth Day of August, 2005



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Director of the United States Patent and Trademark Office